REMARKS

Claims 1-37 are currently pending in the subject application, and are presently under consideration. Claims 1-37 stand rejected. Claims 1, 2, 3, 4, 5, 7, 9, 10, 11, 12, 15, 16, 18, 20, 21, 22, 23, 24, 25, 29 and 30 have been amended and claims 17 and 19 have been cancelled.

Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Interview Summary

Representative for Applicant thanks Examiner Rahman for the courtesy extended during a telephone interview on May 12, 2006. In the interview, Representative for Applicant and Examiner discussed U.S. Patent Application No. 2002/0168043 to Sander relative to the pending claims. While no specific agreements were reached regarding the patentability of the pending claims, the exchange of information was helpful in understanding the Office Action and how the instant application was perceived by the Examiner. The following response is written based upon the discussions with the Examiner during the above-mentioned telephone interview.

II. Rejection of Claims 1-4, 11, 12, 15-18, 24-32, 34-35 under 35 U.S.C. 102(e)

Claims 1-4, 11, 12, 15-18, 24-32, and 34-35 stand rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent Application No. 2002/0168043 to Sander ("Sander"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Regarding claim 1, the Office Action contends that Sander discloses a summation element 409 that corresponds to a detector that provides an indication of a frequency for the input signal based on a signal 403 that is derived from an unknown clock signal Fx (referring to paragraphs [0023] and [0029] and [0030] and Figs. 4 and 5 of Sander). Applicant respectfully traverses the rejection of claim 1.

Claim 1 has been amended to recite a detector that determines the frequency of the input signal based on plural samples of the input signal state for different time instances of the input signal residing within less than or equal to one period of the input signal. Amended claim 1 also recites that the detector provides a value that represents the determined frequency of the input signal.

In contrast to amended claim 1, the summation element 409, as taught by Sander, does not determine the frequency of the input signal based on plural indications of the input signal state for different time instances of the input signal residing within less than or equal to one period of the input signal, as recited in claim 1. As admitted in the Office Action, Sander teaches an input section 401 that produces a derived clock signal having a period that is eight times the unknown clock signal Fx. Office Action at top of page 3, Sander at paragraph [0023]. The derived clock signal 403 (not a sample of the input signal Fx) is provided to an arrangement of logic chains 405 that operate as positive edge transition detectors. For instances, if a positive edge is detected, an output of 1 is provided and if no positive edge is detected an output of 0 is provided. Sander at paragraph [0025]. Each of the logic chains 405 receives a sample of a derived input signal having eight times the period of the input signal to provide different versions of the derived clock signal (via flip flops 405a) for each of the logic chains. Sander at paragraph [0026]. Accordingly, the summation element 409 does not receive plural samples of the input signal state for different time instances of the input signal residing within less than or equal to one period of the input signal, as recited in amended claim 1.

Additionally, summation element 409 of Sander does not determine a frequency value as recited in amended claim 1. Sander teaches that the sum value provided by the summation element 409 provides a measure of the number of transitions of the set of delayed clock signals occurring within a given period of the known clock signal Fs. Sander at paragraph [0029], lines 6-9. Moreover, the decision logic compares the sum value with an alias value, but still only provides a logic output (i.e., a logic 1 or 0) that indicates whether the unknown clock signal Fx is within an octave (corresponding to an expected frequency range). See Sander at paragraphs [0013] and [0029]-[0030]. Since Sander fails to teach or suggest a system that includes a detector as recited in amended claim 1, Sander does not anticipate amended claim 1.

For at least these reasons, Applicant respectfully requests reconsideration and allowance of amended claim 1 as well as claims 2-14 that depend from claim 1.

Claim 2 has been amended to be consistent with the amendment to claim 1. The Office Action contends that flip flops 405e correspond to a plurality of storage elements recited in amended claim 2. However, in contrast to amended claim 2, the flip flops 405e do not provide samples of an input signal Fx to the summation element 409. Instead, as mentioned above, the sum value provided by the summation element 409 provides a measure

of the number of transitions of the set of delayed clock signals occurring within a given period of the known clock signal Fs. Sander at paragraph [0029], lines 6-9. Accordingly, claim 2 is not anticipated by Sander. Claim 11 should be patentable for similar reasons.

The Office Action contends that flip flops Q3-Q6 correspond to delay elements of claim 3. Claim 3 has been amended to recite explicitly that which was believed to be implicit as well as to be consistent with amended claim 1. Amended claim 3 recites that delay elements provide delayed clock signals to clock the at least a substantial number of the storage elements to sample the input signal at different time intervals and thereby provide the plural samples of the input signal. In sharp contrast, Sander discloses outputs of the D flip flops Q3-Q6 are connected to the inputs of flip flops Q7, Q11, Q15 and Q19. The known clock signal Fx is not provided to the clock flip flops Q7, Q11, Q15 and Q19, but instead delayed versions of a derived clock signal having a period greater than the unknown clock signal Fx are provided to the D-inputs of flip flops Q7, Q11, Q15 and Q19. See Sander at paragraphs [0023] and [0025]. Each of Q7, Q11, Q15 and Q19 is clocked by the same known clock signal Fs. See Sander, Fig. 5. Because Sander fails to teach or suggest delay elements that provide respective clock signals to clock the storage elements to sample the input signal at different time intervals, Sanders also fails to teach or suggest that plural samples of the input signal state are also provided to a detector (*e.g.*, the summation element 409). For at least these reasons, Applicant respectfully request reconsideration and allowance of amended Claim 3.

Claim 4 has been amended to be consistent with amended claim 3. As discussed with respect to claim 3, neither the unknown clock signals Fx nor the known clock signal Fs disclosed in Sander is delayed by delay elements. Instead, Sander teaches that Fx is provided directly to clock the D flip flops Q3-Q6 and that Fs is provided directly to clock flip flops Q7-Q22. Accordingly, reconsideration and allowance of amended claim 4 are respectfully requested.

Claim 12 has been amended to be consistent with amended claim 1. As mentioned above with respect to claim 1, Sander does not disclose a detector that determines the frequency of the input signal and provides a value that represents the determined frequency, as recited in amended claim 1. Because of such deficiencies, Sander similarly does not include a comparator that compares the frequency value (provided by the detector of claim 1) with a value of a desired frequency. Instead, Sander discloses that decision logic provides a digital output signal (either a 0 or 1) that forms a number stream for frequency and/or phase

comparison of digital or digitized signals, where typically one of the clock signals is a known clock signal and the other is an unknown clock signal. See Sander, Fig. 4 and at paragraph [0013]. This comparison is based on a sum value for the number of transitions relative to an alias that can be regarded as an octave selection value. See Sander at paragraphs [0025-0027] and last sentence of paragraph [0029].

The Office Action also contends that "[a] controller must be present to implement the adjustment of input clock signal based on comparison of sum with alias." Office Action, at page 4. In contrast to such contention, Sander does not mention a controller for adjusting the unknown signal Fx, but instead simply forms an output number stream as discussed above. Sander fails to teach or suggest a controller to implement adjustments to a clock signal, as suggested in the Office Action, based on the comparison signal. For instance, Sander teaches that the unknown input signal Fx may be derived from a communication signal. Sander at paragraph [0013]. Therefore, it is purely speculation that such a controller would be present in the system of Sander or that the output stream would be used by a controller. For at least these reasons, the Applicant respectfully request that the rejection of Claim 12 be withdrawn.

Claim 15 has been amended to recite that storage elements are clocked by respective clock signals to latch different time instances of an input signal to provide corresponding output samples sufficient for determining a frequency value of the input signal. Claim 15 has also been amended to substantially incorporate the subject matter of claim 17, reciting delay elements that provide the respective clock signals. Accordingly, the following remarks address the issues presented in the Office Action with respect to claims 15 and 17.

In contrast to amended claim 15, Sander fails to disclose that storage elements are clocked to latch in different time instances of the input signal to provide corresponding output samples of the input signal. Instead, in Sander, previous states of D flip flops Q7, Q11, Q15 and Q19 are latched into other D flip flops at times determined simultaneously by the combination of a known clock signal Fx, and an unknown clock signal Fs. See Sander at paragraph [0023]. Additionally, the output samples from Q10, Q14, Q18 and Q22 do not correspond to samples of the derived clock signal that is sampled by Q7, Q11, Q15 and Q19. As discussed above, the outputs of Q10, Q14, Q18 and Q22 indicate whether there has been a positive edge transition of the unknown clock signal Fx within a given period of the known clock signal Fs. See Sander at paragraphs [0025] and [0029]. In contrast to amended claim 15, Q10, Q14, Q18 and Q22 do not provide samples of the input signal Fx, as suggested in the Office Action.

Moreover, Sander fails to teach delay elements that provide respective clock signals for clocking storage elements to latch respective ones of the different time instances of the input signal for providing the corresponding output samples, as recited in amended claim 15. The Office Action contends that Q7, Q11, Q15 and Q19 correspond to storage elements of claim 15, which flip flops are clocked by the same known clock signal Fs. See Sander at Figure 5 where Fs is applied to the clock inputs. However, the flip flops Q3-Q6 provide output signals to the D-inputs of Q7, Q11, Q15 and Q19, respectively. Additionally, Q3-Q6 do not provide samples of the known clock signal Fx to Q7, Q11, Q15 and Q19, but instead Q3-Q6 provide to Q7, Q11, Q15 and Q19 samples of a derived clock signal having a period greater (*e.g.*, eight times greater) than the unknown clock signal Fx. See Sander at paragraphs [0023] and [0025]. Q7, Q11, Q15 and Q19 are all clocked by Fs. From this arrangement, Sander fails to teach that the respective clock signals from the delay elements clock at least a substantial number of the storage elements to latch a respective one of the different time instances of the input signal to provide at least a portion of the corresponding output samples, as recited in amended claim 15.

For these reasons, the Applicant respectfully request reconsideration and allowance of amended claim 15 as well as claims 16, 18, and 20-24, which depend from claim 15. Claims 17 and 19 have been cancelled.

Regarding amended claim 16, similar to as discussed with respect to claim 1, Sander fails to teach or suggest a detector provides a frequency value based on output samples (of the input signal) that correspond to different time instances of the input signal residing within a single period of the input signal detector. Reconsideration and allowance of amended claim 16 are respectfully requested.

Claim 18 has been amended to be consistent with the amendment to claim 15 from which it now depends. The Office Action contends that Q3-Q6 are delay elements that delay the unknown clock signal Fx for activating flip flops Q7, Q11, Q15 and Q19. However, as discussed above with respect to claim 15, the outputs of Q3-Q6 do not provide clock signals that clock the Q7, Q11, Q15 and Q19, but instead provide delayed versions of a derived clock signal 403 to the D-inputs of Q7, Q11, Q15 and Q19. Moreover, the unknown signals do not correspond to different time instances of the unknown signal Fx, but are generated by propagating the derived clock signal that is generated from Fx through a series of interconnected flip flops Q3-Q6. Accordingly, Sander fails to teach that storage elements are clocked to latch the different time instances of the input signal into storage elements, as

recited in amended claim 18. For at least these reasons, Applicant respectfully requests reconsideration and allowance of amended claim 18.

Claim 24 has been amended to recite that the storage elements are clocked by the respective clock signals (provided by the delay elements of claim 1) at predetermined time intervals to latch the output samples to the detector concurrently to provide the corresponding output samples. In contrast, Sander does not teach that storage elements are clocked by clock signals at predetermined times to provide the corresponding output samples that represent different time instances of the input signal state. Instead, Sander teaches that Q7, Q11, Q15 and Q19 are clocked by the known clock signal Fs to shift in the multiphase divided set of signals into such flip flops. See Sander Figs. 5 and 6, and at paragraph [0032]. For at least these reasons, Applicant respectfully requests reconsideration and allowance of claim 24.

Claim 25 has been amended to correct typographical errors and to make explicit that which was previously implicit. The means for determining of claim 25 has also been amended to recite that the frequency is determined based on the plural indications of signal state that correspond to time instance of the input signal residing within a single period of the input signal. Means for providing a corresponding frequency value for the determined frequency has also been added to the system of claim 25. Claim 25 is not anticipated by Sander for reasons similar to those stated above with respect to claim 1. Reconsideration and allowance of amended claim 25 are respectfully requested.

Claim 27 is dependent upon Claim 25 and should be allowable over Sander at least for the reasons stated for Claim 25. In Sander, no clock signals are delayed, but instead the two clocks Fx, and Fs are used to clock the D flip flops (Q3-Q6 and Q7, Q11, Q15 and Q19) in Sander without delay. For at least these reasons, Applicant respectfully requests reconsideration and allowance of claim 27.

Claim 28 is dependent upon Claim 25 and should be allowable over Sander at least for the reasons stated for Claim 25. The system of Sander does not include means for storing signal state information, but instead produces new derived clock signals relative to an unknown signal Fx, which derived clock signals are clocked by the known clock signal Fs. See Sander at paragraph [0025] and Fig. 5. The system in Sander does not samples signals, but instead changes the state of interconnected D flip flops. In Sander, the D-inputs of the flip flops are not connected to the signal input signals, Fx or Fs, so input state information of

input signals can not be stored. For at least these reasons, the Applicant respectfully request that the rejection of Claim 28 be withdrawn.

Claim 29 is dependent upon Claim 28 and should be allowable over Sander at least for the reasons stated in Clam 28. Additionally Sander does not teach that a controller will control the frequency of an input signal based on the comparison of the frequency of the input signal and desired signal. For at least these reasons and those stated above with respect to claim 12, Applicant respectfully requests that the rejection of Claim 29 be withdrawn.

Claim 30 has been amended to recite that the determination of a frequency value for the sampled signal is based on output samples that correspond to time instances of the signal residing within a single period of the input signal. In contrast, the Sander does not teach that a signal is sampled as recited in claim 30, but instead an input section produces a derived clock signal having a period that is eight times greater than the unknown clock signal Fx. See Sander at paragraph [0023]. Delayed versions of this derived signal are clocked into flip flops Q7, Q11, Q15 and Q19 by the known clock signal Fs. See Sander at Fig. 5 and at paragraph [0025]. Moreover, for substantially the same reasons discussed above with respect to claim 1, Sander does not disclose that a frequency value for the sampled signal is determined based on output samples that correspond to time instances of the signal residing within a single period of the signal as recited in claim 31. For instance, Sander teaches that each of Q3-Q6 are clocked by the unknown signal Fx, such that there cannot be time instances of the signal within a single period of the sample based on which the frequency value is determined as recited in amended claim 30. Accordingly, Applicant respectfully requests reconsideration and allowance of amended claim 30 as well as claims 31-37 that depend from claim 30.

III. Rejection of Claim 5, 6, 14, and 20 under 35 U.S.C. 103(a)

Claims 5, 6, 14, and 20 stand rejected under 35 U.S.C. 103(a) as unpatentable over Sander. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 5 has been amended for sake of consistency with the amendments to claim 1. The Office Action takes Official Notice that an oscillator is well known in the art and then concludes that it would be obvious to use such an oscillator to provide the clock signal. However, as discussed above with respect to claims 1 and 2, Sander does not teach or suggest that the clock signal Fs, regardless of where it might be generated, activates storage elements

to provide plural indications of the input signal state to a detector, as recited in amended claim 5. Instead, Sander teaches that Q1-Q6 produce a sequence of delayed versions of the derived clock signal (having a period that is eight times that of the unknown clock signal Fx). See Sander at paragraph [0029]. For these reasons and for those stated above with respect to claims 1 and 2, Applicant respectfully requests reconsideration and allowance of amended claim 5.

Claim 20 has been amended to be consistent with the amendments to claim 15 and to make explicit that which was implicit. Sander fails to teach or suggest that the oscillator provides the sample signal to delay elements based on which the respective clock signals are provided for latching different time instances of the input signal into the plurality storage elements. As discussed above, the same known clock signal Fs is provided directly to each of Q7, Q11, Q15 and Q19 without delay for latching the delayed versions of the derived clock signal 403. See Sander, Fig. 4 and at paragraphs [0023] and [0029]. There is not proper motivation or suggestion to delay the known clock signal Fs as is being suggested in the Office Action to latch different time instances of the input signal, as in amended claim 20. Therefore, claim 20 should be patentable for these reasons as well as those discussed above with respect to amended claim 15.

Claim 6 is dependent upon amended claim 5 and should be allowed at least for the reasons stated for Claim 5.

Claim 14 is dependent upon amended claim 1 and should be allowed at least for the reasons stated for Claim 5

IV. Rejection of Claim 7-10, 19, 21-23, and 33 under 35 U.S.C. 103(a)

Claims 7-10, 19, 21-23, and 33 stand rejected under 35 U.S.C. 103(a) as unpatentable over Sander in view of U.S. Patent 6,326,826 to Lee et al ("Lee et al."). Withdrawal of this rejection is respectfully requested for at least the following reasons. The addition of Lee fails to overcome the deficiencies of Sander discussed above.

Additionally, claim 7 has been amended to be consistent with the amendments to claim 1 as well as to recite that the delay elements each has a fixed amount of delay for providing the respective clock edges. In addition to reasons stated above regarding Claim 5, the delay elements taught by Lee do not provide fixed amount of delay for providing the respective clock edges. Lee teaches that each of the delay elements is variable to control the amount of delay depending on the number of edges detected relative to a predetermined

number of clock edges. Lee at Col. 2, lines 3-9. Applicant also traverses the contention that it would be obvious to combine the system of Sander with the system of Lee et al. to create the system of Claim 7, as suggested in the Office Action. For example, the Office Action states as motivation for the purported combination because the "arrangement of delayed locked loop can operate over a wide frequency range and provide protection against false locking." Office Action at page 9. However, the purported teachings in the combination of Sander and Lee fails to teach or suggest that plural samples of an input signal state for different instances of an input signal. For example, Lee fails to teach or suggest that samples of an input signal state are provided, as recited amended claim 7. Instead, Lee teaches that a frequency divider is used to derive an extended version of a reference clock and the extended version of the reference clock is delayed to provide a multi-phase clock signal CK[N]. Lee at Col. 3, lines 6-12. The states of such multiphase clock are not samples of an input signal state, as recited in claim 7, but instead correspond to rising edges triggered by the rising edge of the divided-by-2 version of the reference clock signal that propagates through the delay elements 18'. See Lee Fig. 1 and at Col. 3, lines 6-10. Lee further teaches that the amount of delay is varied so as to adjust the frequency of the multiphase clock signal so as to achieve a frequency lock; namely, assuming 7 delay cells, each delay cell should be set to delay the reference clock by $1/7^{th}$ of the reference clock. See Abstract of Lee and Fig. 3 and corresponding description at Col. 3, lines 29+. That is, Lee teaches an approach to determine and control the amount of delay implemented by the respective delay elements for providing a multiphase clock signal that is locked relative to a reference clock signal. Significantly, this is disclosed in Lee without providing samples of an input signal state. Accordingly, even when the teachings of Lee are combined with Sander, the combination fails to teach or suggest the system recited in claim 7. Therefore the Applicant respectfully requests that the rejection of Claim 7 be withdrawn.

Claim 8, is dependant on Claim 7, which is should be patentable over the system of Sander in combination of the system of Lee et al. at least for the reasons provided for Claim 7. Therefore, the applicant asks that the rejection of claims 8 be respectfully withdrawn.

Claim 9 has been amended to depend from claim 2 and thus should be patentable for at least the same reasons stated above with respect to claim 2.

Claim 10 has been amended to recite that the input signal is provided directly to the input of each of the storage elements. As discussed in the Office Action with respect to claim 1, Sander teaches that the unknown clock signal Fx clock the D flip flops, which are coupled

in series, Q output to D input, so as to form a ring. Sander at paragraph [0023]. Accordingly, Sander does not teach or suggest providing the input signal directly to the input of each storage elements, as recited in amended claim 10. Additionally, in Sander, the delayed versions of derived clock signal having a period that is greater than the unknown clock signal Fx are input into the clock input of D flip flops Q7, Q11, Q15, and Q19. That is Sander teaches that, the outputs of Q3, Q4, Q5 and Q6 (corresponding to versions of the derived clock signal 403) are provided to the inputs of the D flip flops Q7, Q11, Q15 and Q19, respectively, based on the known clock signal Fs clocking each of Q7, Q11, Q15, and Q19. In Sander, no sample of the signal Fx is stored in any flip flop and provide output samples Sum based on activation by the clock edge Fs, as appears is being suggested in the Office Action. Additionally, the Office Action fails to provide information about how the teachings of Lee can be combined with the teachings of Sander to create the system of Claim 10. Moreover, it would not be obvious to combine the system of Sander with the system of Lee et al. to create the system of Claim 10 since the use of the flip flops Q7, Q11, Q15 and Q19 of Sander with the teachings of Lee in view of the significantly different approaches and purposes taught in Sander and Lee. For at least these reasons, Applicant respectfully requests reconsideration and allowance of Claim 10.

Claims 21-23 should be patentable for at least the same reasons as claim 20 and 15 from which they depend. Claim 23 also is patentable over Lee and Sander for reasons similar to those discussed above with respect to claim 10.

V. Rejection of Claim 13, 36 and 37 under 35 U.S.C. 103(a)

Claims 13, 36, and 37 stand rejected under 35 U.S.C. 103(a) as unpatentable over Sander in view of U.S. Patent Application Publication 2004/0139363 to Elbe et al. ("Elbe et al."). Withdrawal of this rejection is respectfully requested for at least the following reasons. The addition of Elbe et al. fails to over the deficiencies of Sander discussed above.

The Office Action cites Elbe et al. as a general teaching of an oscillator that generates an input signal as a clock signal having a frequency based on a controller output signal. Office Action at page 11. Applicant traverses that it would have been obvious to combine such a teaching with the teachings of Sander to create the subject matter of claim 36. As discussed above, Sander does not mention a controller for adjusting the unknown signal Fx, but instead simply forms an output number stream as discussed above. Significantly, Sander teaches that the unknown input signal Fx may be derived from a communication signal.

Sander at paragraph [0013]. That is, since Sander teaches that the input signal Fx of Sander is an unknown clock signal that is input to the system of Sander, it would seem contrary to rational reasoning to suggest that it would be obvious to control an oscillator in the system of Sander (based on Elbe et al.) to generate the input signal Fx at a frequency based on a comparison of the indication of frequency of the signal relative to a desired frequency, as recited in claim 36. Such a conclusion requires motivation that far exceeds that stated in the Office Action, as the suggested combination would require that the unknown input signal Fx be known (contrary to the teaching of Sander). Accordingly, reconsideration and allowance of claims 36 and 37 are requested.

VI. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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